Gavin O'Hara

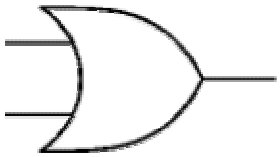
## Task 1

**For each of the gates listed below, explain their operation showing appropriate gate symbols, truth tables and logic equations for the outputs in terms of the input variables.**

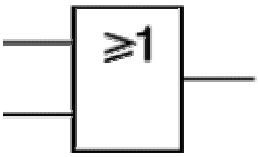
### a) Two input OR gate

Logic gates process signals which represent **true** or **false**. Normally the positive supply voltage +Vs represent true and 0V represents false. Other terms which are used for the true and false states are shown in the table on the right. It is best to be familiar with them all.

**The output Q is true if input A OR input B is true (or both of them are true): Q = A OR B**
**An OR gate can have two or more inputs, its output is true if at least one input is true.**



**Traditional symbol**




**IEC symbol**

| Input A | Input B | Output Q |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

**Truth Table**

### b) Two input AND gate

The AND gate is a digital logic gate that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results.

| AND |  |  | $A \cdot B$ |
|---|---|---|---|

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A AND B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

### c) Two input NAND gate

NAND gates are one of the two basic logic gates (along with NOR gates) from which any other logic gates can be built. Due to this property, NAND and NOR gates are sometimes called "universal gates". However, contrary to popular belief, modern integrated circuits are not constructed exclusively from a single type of gate.

| NAND |  |  | $\overline{A \cdot B}$ |
|---|---|---|---|

| INPUT | | OUTPUT |
|---|---|---|
| A | B | A NAND B |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

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## Task 2

For this task I built a circuit that lights up a bulb when 2 or more inputs are detected. I built this circuit on a circuit board, and used a variety of components, as well as a power supply. I then used a logic probe to test the circuit, to see if it was functioning properly. Below is the truth table for this circuit

| **A** | **B** | **C** | **Z** |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

## Task 4

For this task I was required to modify the drawings that I produced using workbench. I modified it to turn it into an active low circuit. For this, I basically just changed the OR gate to a NOR gate. This makes the output the complete opposite of the original Boolean equation. I have produced 2 printouts of this from workbench.

Boolean equation, for the standard circuit

$Z = A.B.C + A.B.C + A.B.C + A.B.C$

Active low equation, we use the NOR gate

$Z = A.B.C + A.B.C + A.B.C + A.B.C$

| A | B | C | Z |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

**Task 5**

For this task I was asked to produce a minimized circuit. I did this by using the karnaugh map below.

| BC<br>A | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | | | 1 | |
| 1 | | 1 | 1 | 1 |

The minimized equation for this circuit is:

A.B + A.C + B.C

I built this circuit, using the same equipment as previous, such as the logic probe etc. this circuit does the function as the original circuit, but only this time there are less components used. This has many benefits, as it makes the entire circuit cheaper to build, and the person building the circuit is less likely to make a mistake in the construction of it.

**Task 6**

**Compare and contrast, with reference to five characteristics the differences between the 2 types of logic family listed below.**

TTL chips are somewhat less sensitive to static so they are safer to handle and easier to interface to external connections. CMOS has additional modes of operation not available in TTL, ie buffers can act linear as amplifiers.

It uses a multi emitter transistor, a transistor with many emitter terminals. As every emitter is nothing but a diode, this logic eliminates the use of all diodes. This is the major advantage. A transistor turns ON and OFF much more rapidly than a diode, and switching time will also be faster.

TTL, or Transistor-transistor logic replaced resistor-transistor logic, and uses much less power. The TTL family is very fast, reliable, and less power consuming.

CMOS has good packing density. TTL takes up more space CMOS has better noise immunity. TTL has a smaller noise immunity range CMOS has a large fan out. TTL can power fewer inputs CMOS consume less power. TTL use more power CMOS are highly static sensitive. TTL IC's tend to be less susceptible to static electricity CMOS uses FETS (Field-Effect Transistors) TTL uses BJTs (Bipolar junction Transistors CMOS can run with a range of supp
ly voltages. TTL IC's run with a 5V supply. CMOS uses Vdd and Vss for it's power connections TTL uses BJTs (Bipolar junction Transistors

CMOS takes a lot less power and is therefore suitable for battery applications, but generally speaking can't run as fast. TTL devices can drive more power into a load. CMOS chips can be damaged by static electricity: even a static jolt that you or I can't feel might destroy a CMOS chip.

I have been asked to compare 5 characteristics of TTL and CMOS. I have chosen a component for each sector and I will compare their statistics.

In the TTl component the propagation delay time ranges from 27-19 ns. On the CMOS, the delay ranges from 95-40ns. The propagation delay time, is the time it takes to send the signal from the sender to the receiver. TTL would be the best suited for changing signal outputs quickly.

The TTL supply current ranges from 11-33mA. CMOS ranges from 1-30A. the CMOS chip requires less amps to operate, so for it would be better suited for low power circuits.
The TTL needs 4.75-5.25V, whilst CMOS chip requires between 3-15V. this means the CMOS chip would be the best for altering voltage. This makes CMOS the most useful.

TTL can operate at a temperature range of 0-70C. The CMOS chip again beats this, because it has a superior temperature operating range of -40-+85C. CMOS wins this because it is best suited to large temperature changes.

The high level output voltage on the TTL chip is 2.4v, whilst the CMOS has an output voltage, of 2 thirds that of the input voltage. E.g. if the input voltage is 5V, the output is 3.333V.

In conclusion I feel that the CMOS chip is the superior chip for today's demands. The only area that CMOS is outperformed by TTL is the Propagation Delay Time. This means CMOS is a great chip.